What is claimed is:

1. A semiconductor memory device comprising:

a first memory block and a second memory block, each memory block including a bitline pair;

a sense amplifier provided between the first memory block and the second memory block;

bitline isolation circuits for selectively connecting the first memory block and the second memory block to the sense amplifier in response to a first bitline isolation signal and a second bitline isolation signal;

bitline equalizing circuits for providing bitline precharge voltage to the bitline pair in response to a first bitline equalizing signal and a second bitline equalizing signal; and

a bitline equalizing voltage generator for generating bitline equalizing voltage by utilizing a voltage of the bitline isolation signals.

2. A semiconductor memory device according to the claim 1, wherein the bitline equalizing voltage generator comprising:

a first controller driven by a boost voltage level and generating a first control signal in response to a first block selection signal and a second block selection signal;

a second controller driven by an external voltage level and generating a second control signal in response to the first control signal;

an equalizer for generating the first bitline isolation signal and the second bitline isolation signal in response to the first control signal;

a driver for driving the first bitline isolation signal and the second bitline isolation signal in response to the second control signal; and

a transfer circuit for providing a half level of the equalized bitline isolation signal as bitline equalizing voltage when the first bitline isolation signal and the second bitline isolation signal are deactivated.

3. A semiconductor memory device according to the claim 1, wherein the memory device further comprising:

a bitline equalizing signal generator and a second bitline equalizing generator for selectively generating the first bitline equalizing signal and the second bitline equalizing signal fed from the bitline equalizing voltage or the external voltage in response to a first memory block selection signal and a second memory block selection signal.

4. A semiconductor memory device according to the claim 3, wherein the bitline equalizing signal generator comprising:

a first driver for providing the first bitline equalizing signal and the second bitline equalizing signal with the bitline equalizing voltage level in response to the first memory block selection signal and the second memory block selection signal; and

a second driver for providing the first bitline equalizing signal and the second bitline equalizing signal with the external voltage level in response to the first complement memory block selection signal.

5 . A semiconductor memory device having a plurality of memory blocks comprising:

a sense amplifier provided between a first memory block and a second memory block;

bitline isolation circuits for selectively connecting the first memory block and the second memory block to the sense amplifier in response to a first isolation signal and a second bitline isolation signal;

bitline equalizing circuits for providing bitline precharge voltage to the bitline pair in response to a first bitline equalizing signal and a second bitline equalizing signal; and

a bitline equalizing voltage generator for connecting bitline equalizing voltage by utilizing a voltage of a word line drive signal.

6. a semiconductor memory device according to the claim 5, wherein the bitline equalizing voltage generator comprising:

a word line drive signal generator for generating the word line drive signal having a boost voltage level in response to a word line drive signal provided by a row decoder; and

a bitline equalizing voltage driver for serving the word line drive signal as the bitline equalizing voltage in response to a word line drive pulse signal which is generated in response to the bitline precharge and the word line address signal.

7. A semiconductor memory device according to the claim 6, wherein the bitline equalizing voltage driver comprising:

a first pmos transistor, a gate thereof being supplied the word line drive pulse signal, a source thereof being supplied the word line drive signal; and

a second pmos transistor, a gate thereof being supplied the bitline precharge voltage, a drain thereof being supplied the bitline equalizing voltage, a source thereof being connected to the drain of the first pmos transistor.

8. A semiconductor memory device having a plurality of memory blocks:

a bitline equalizing voltage generator generating a bitline equalizing voltage coupled to a bitline equalizing signal by recycling boost voltage of the bitline isolation signal;

an external voltage detector generating a first enable signal by comparing an external voltage with a reference voltage;

a bitline equalizing voltage detector generating a second enable signal by comparing the bitline equalizing voltage with a bitline precharge voltage;

an oscillator generating an oscillation signal in response to the first enable signal and the second enable signal;

a charge pumping circuit pumping the external voltage into the bitline equalizing voltage; and

a switching circuit coupling the external voltage with the bitline equalizing voltage in response to the first enable signal.

9. A semiconductor memory device according to the claim 8, wherein the external voltage detector comprising:

a voltage divider having a first to a third resistors which are serially connected between external voltage and ground voltage, wherein the first resistor is connected to a transistor at its both ends and a gate of the transistor receives a first enable signal;

a comparator comparing a reference voltage with a node voltage between the second and the third resistor of the voltage divider; and

a driver receiving the output of the comparator and generating the first enable signal.

10. A semiconductor memory device according to the claim 8, wherein the bitline equalizing voltage detector comprising:

a voltage down converter having a diode connected nmos transistor and a resistor which are serially connected between the bitline equalizing voltage and a ground voltage;

a comparator comparing the bitline precharge voltage with a node voltage between the NMOS transistor and the resistor; and

a driver receiving the output of the comparator and generating the second enable signal.